****Dayananda Sagar College of Engineering

**Department of Electronics and Communication Engineering**

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**(An Autonomous Institute affiliated to VTU, Approved by AICTE & ISO 9001:2008 Certified)**

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**AAT**

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| Program: B.E. | Branch: ECE |
| Course: Fundamentals of Analog VLSI Design | Semester/Section : 6th Sem ‘D’ |
| Course Code: 19EC6DCFOV | Date: 18-06-2022 |

**A Report on**

**8 BIT CARRY LOOK AHEAD ADDER**

**Submitted by**

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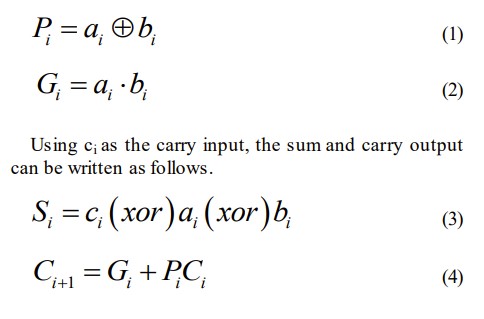
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* **INTRODUCTION :**

Carry look ahead adder is an electronic adder also called as fast adder, it is used in digital logic. For an integrated circuit design, the performance and other parameters are important for designing. Binary addition is a popular methodology among computational logic elements. There are lots of ways of implementing the binary addition. Encoding, replication of common factors and pre-charging are some of them. Also the same functional block can be implemented using different logic approach like static, CMOS, dynamic logic, pass transistor based logic and adiabatic logic etc. Each method is having its own advantage based on simplicity, in terms of area that is related to cost, delay and power consumption. The n -bit adder has n one-bit full adders known as ripple carry adder. In this method the carry is computed. The addition is not complete until the n-1th adder has computed the n-1th output. The carry chain is meant for the total delay of the logic element. Therefore, speeding up the adder needs the speeding up the carry chain. As speed of the addition is the main criteria with nominal amount of power consumption, the carry look ahead adder has been chosen. The carry-look-ahead adder is one way to speed up the carry computation. The carry-look-ahead adder breaks the carry computation into two steps, starting with the computation of two intermediate values. If the adder has two inputs ai and bi , then Pi and Gi can be written as follows.



Expanding the ci , the ci+1 can be generated as a function of inputs and c0

Carry look ahead adder depends on two things that have been explained as follows.

1. Calculating, for each digit position, whether that position is going to propagate a carry if one comes in from the right.

2. Combining these calculated values to be able to deduce quickly whether, for each group of digits, that group is going to propagate a carry that comes in from the right.

Supposing that groups of 4 digits are chosen. Then the sequence of events goes something like this:

1. All 1-bit adders calculate their results. Simultaneously, the look ahead units perform their calculations.

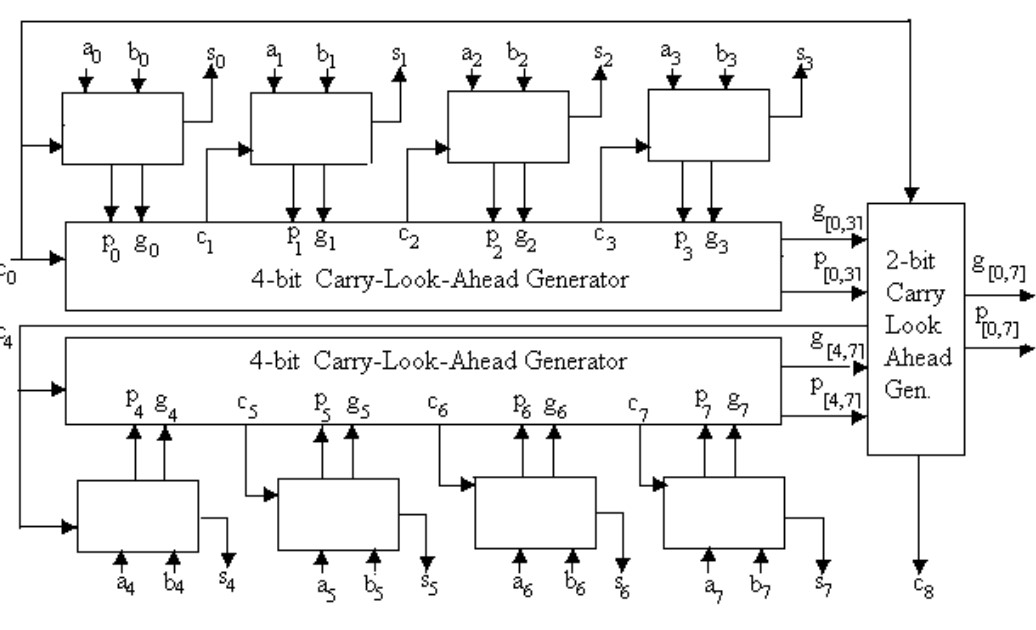
2. Suppose that a carry arises in a particular group. Within at most 3 gate delays, that carry will emerge at the left-hand end of the group and start propagating through the group to its left.

3. If that carry is going to propagate all the way through the next group, the look ahead unit will already have deduced this. Accordingly, before the carry emerges from the next group the look ahead unit is immediately (within 1 gate delay) able to tell the next group to the left that it is going to receive a carry - and, at the same time, to tell the next look ahead unit to the left that a carry is on its way.

Table

Description automatically generated

8 BIT CARRY LOOK AHEAD ADDER



SCHEMATIC VIEW :

Schematic view of 4 bit carry look ahead adder

A screenshot of a computer

Description automatically generated with low confidence

Symbolic representation of 4 bit carry look ahead adder

A screenshot of a computer

Description automatically generated with medium confidence

A picture containing text, electronics

Description automatically generated

Cascaded 8 bit carry look ahead adder

OUTPUTS:

4 BIT CARRY LOOK AHEAD ADDER 1 AND 2

A screenshot of a computer

Description automatically generated with medium confidence

Graphical user interface

Description automatically generatedTable

Description automatically generatedEXAMPLE : AS IN WAVEFORMS

LAYOUT:

A screenshot of a computer

Description automatically generated with low confidence

Power and Delay Calculation:

The power and delay calculation of eight bit CLA has been calculated for 4-bit CLA using Virtuoso tool which using 180 nm technology. Power consumption and delay calculation has been done by simulation result.

Comparitive Analysis:

Table

Description automatically generatedCONCLUSION:

In Electronics, VLSI is one of the broad category. All parameter of the circuit is simulated and Evaluated through Cadence tool. Circuits parameters are simulated at supply voltage of 1V. In this paper, 4-bit CLA consumes less power. Since 8-bit CLA is combination of two 4-bit CLA, it is also consume less power. Thus, the MCLA 8-bit carry look ahead adder have been designed with less power consumption of 61.05uW and with less delay. The results of CLA design reveal that they have acceptable performance for practical applications.

Applications:

• In digital signal processors- CLA is used to reduce the power consumptions and for battery backups in mobile phones and laptops.

• In multipliers- CLA is used to increase the speed and reduce area.

• In filtering process- the carry look ahead adder used in multipliers are used to improve its efficiency.

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